## **S8822 - OPTIMIZING NMT WITH TENSORRT**

Micah Villmow

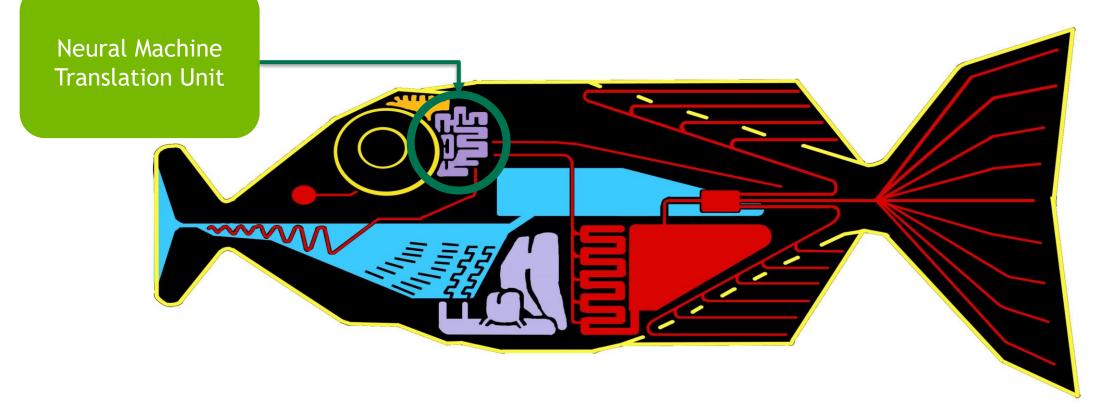
Senior TensorRT Software Engineer

**OVIDIA**.

## 100倍以上速く、 本当に可能ですか?



#### **DOUGLAS ADAMS - BABEL FISH**

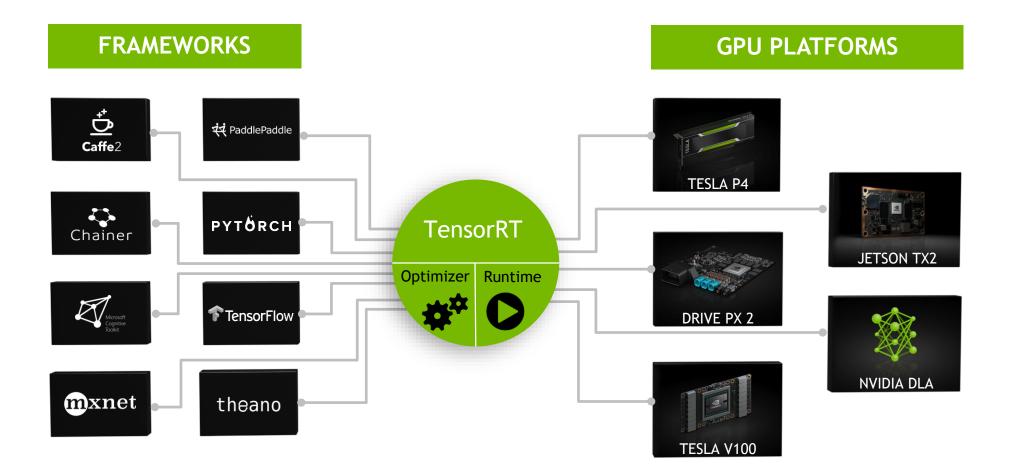


## OVER 100X FASTER, IS IT REALLY POSSIBLE?



#### **NVIDIA TENSORRT**

#### Programmable Inference Accelerator



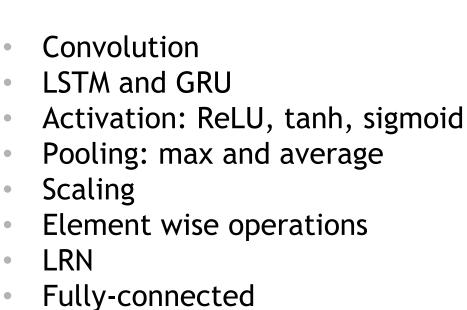
## **TENSORRT LAYERS**

#### Built-in Layer Support

#### **Custom Layer API**

TensorRT Runtime

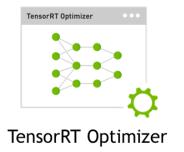
**Deployed Application** 



**Custom Layer** FCPlugin(const void\* data, size\_t length) const char\* d = reinterpret cast const char\*>(data), \*a = d; mKernelWeights = copyToDevice(d+
sizeof(int), \*reinterpret cast<cons</pre> int\*>(d)); d += sizeof(int) + mKernelWeight count \* sizeof(float); mBiasWeights = copyToDevice(d + sizeof(int), \*reinterpret\_cast<const int\*>(d)); d += sizeof(int) + mBiasWeights.com \* sizeof(float); assert (d == a + length) : **CUDA Runtime** 

- SoftMax
- Deconvolution

## **TENSORRT OPTIMIZATIONS**



Layer & Tensor Fusion



Weights & Activation Precision Calibration

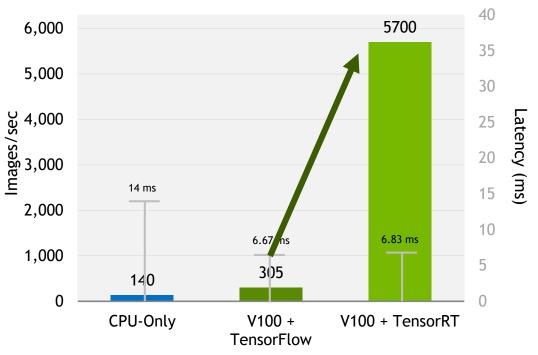


Kernel Auto-Tuning



Dynamic Tensor Memory

#### 40x Faster CNNs on V100 vs. CPU-Only Under 7ms Latency (ResNet50)



Inference throughput (images/sec) on ResNet50. V100 + TensorRT: NVIDIA TensorRT (FP16), batch size 39, Tesla V100-SXM2-16GB, E5-2690 v4@2.60GHz 3.5GHz Turbo (Broadwell) HT On V100 + TensorFlow: Preview of volta optimized TensorFlow (FP16), batch size 2, Tesla V100-PCIE-16GB, E5-2690 v4@2.60GHz 3.5GHz Turbo (Broadwell) HT On. CPU-Only: Intel Xeon-D 1587 Broadwell-E CPU and Intel DL SDK. Score doubled to comprehend Intel's stated claim of 2x performance improvement on Skylake with AVX512.

7 📀 NVIDIA

# Agenda

## • What is NMT?

- What is current state?
- What are the problems?
- How did we solve it?
- What perf is possible?

## **ACRONYMS AND DEFINITIONS**

NMT: <u>N</u>eural <u>M</u>achine <u>T</u>ranslation

OpenNMT: Open source NMT project for academia and industry

Token: The minimum representation used for encoding(symbol, word, character, subword)

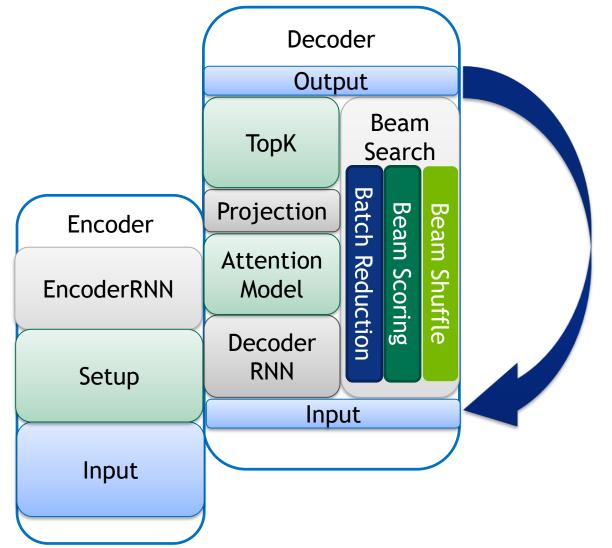
Sequence: A number of tokens wrapped by special start and end sequence tokens.

Beam Search: directed partial breadth-first tree search algorithm

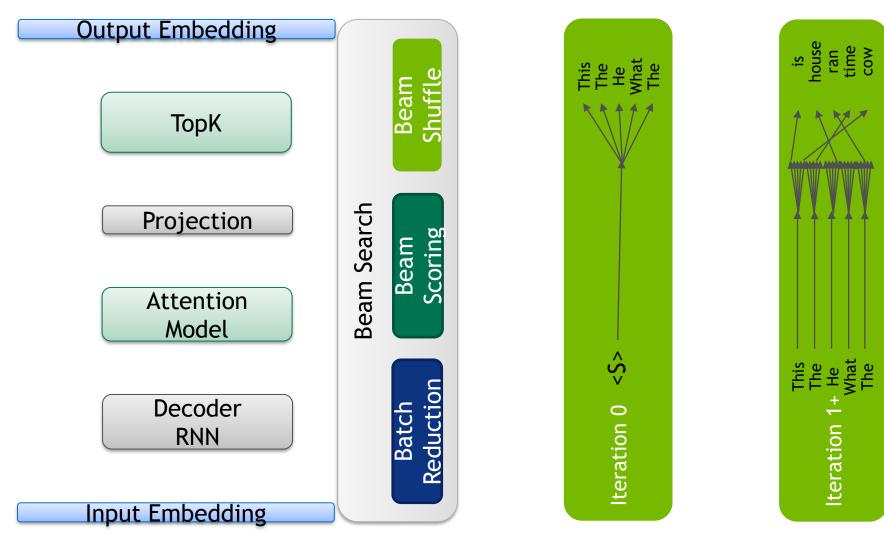
TopK: Partial sort resulting in N min/max elements

Unk: Special token that represents unknown translations.

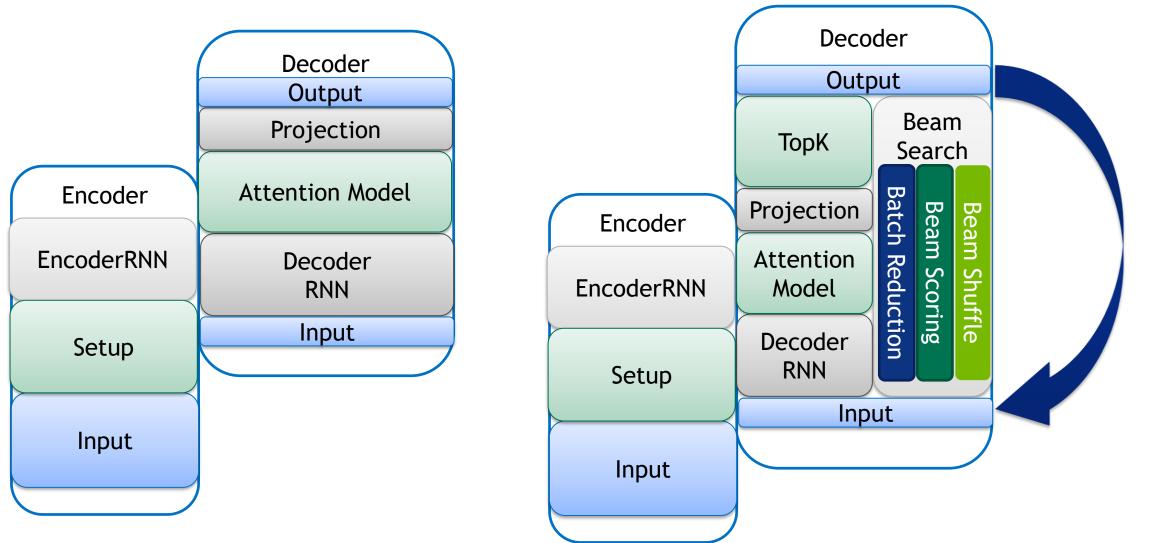
#### **OPENNMT INFERENCE**



#### **DECODER EXAMPLE**



### **TRAINING VS INFERENCE**



# Agenda

- What is NMT?
- What is current state?
- What are the problems?
- How did we solve it?
- What perf is possible?

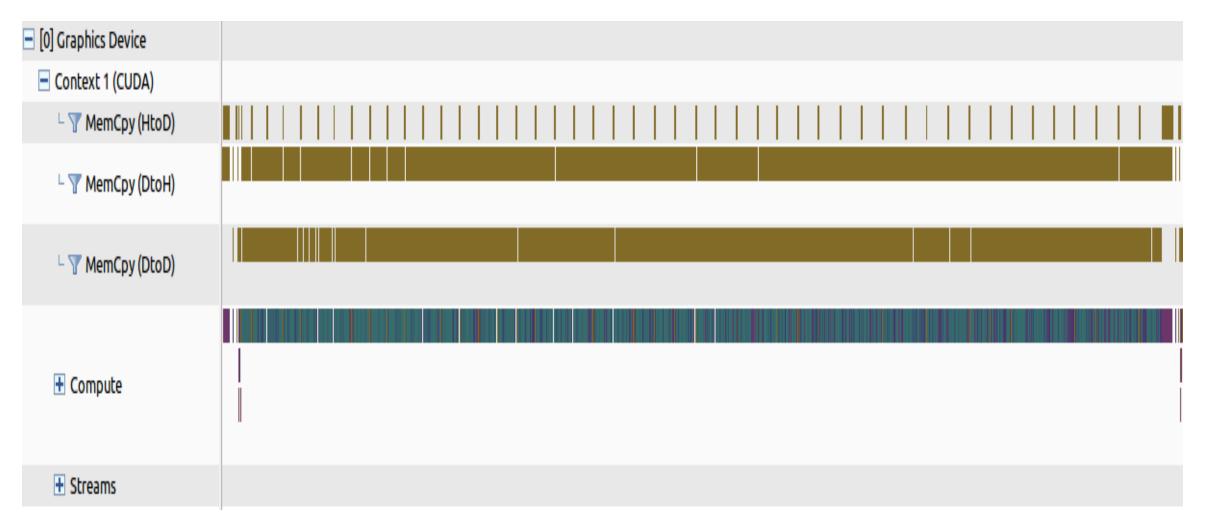
## INFERENCE TIME IS BEAM SEARCH TIME

- Wu, Et. Al. 2016, 'Google's Neural Machine Translation System: Bridging the Gap between Human and Machine Translation' <u>arXiv:1609.08144</u>
- Sharan Narang, Jun, 2017, Baidu's DeepBench https://github.com/baidu-research/DeepBench
- Rui Zhao, Dec, 2017, 'Why does inference run 20x slower than training.' - <u>https://github.com/tensorflow/nmt/issues/204</u>
- David Levinthal, Ph.D., Jan, 2018, 'Evaluating RNN performance across hardware platforms.'

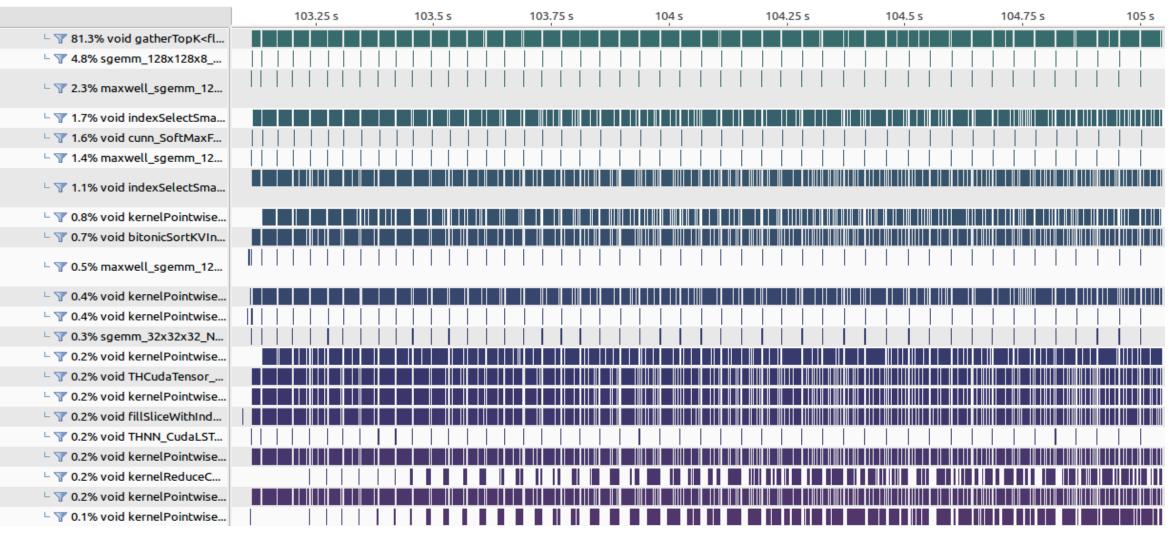
# Agenda

- What is NMT?
- What is current state?
- What are the problems?
- How did we solve it?
- What perf is possible?

### **PERF ANALYSIS**



## **KERNEL ANALYSIS**

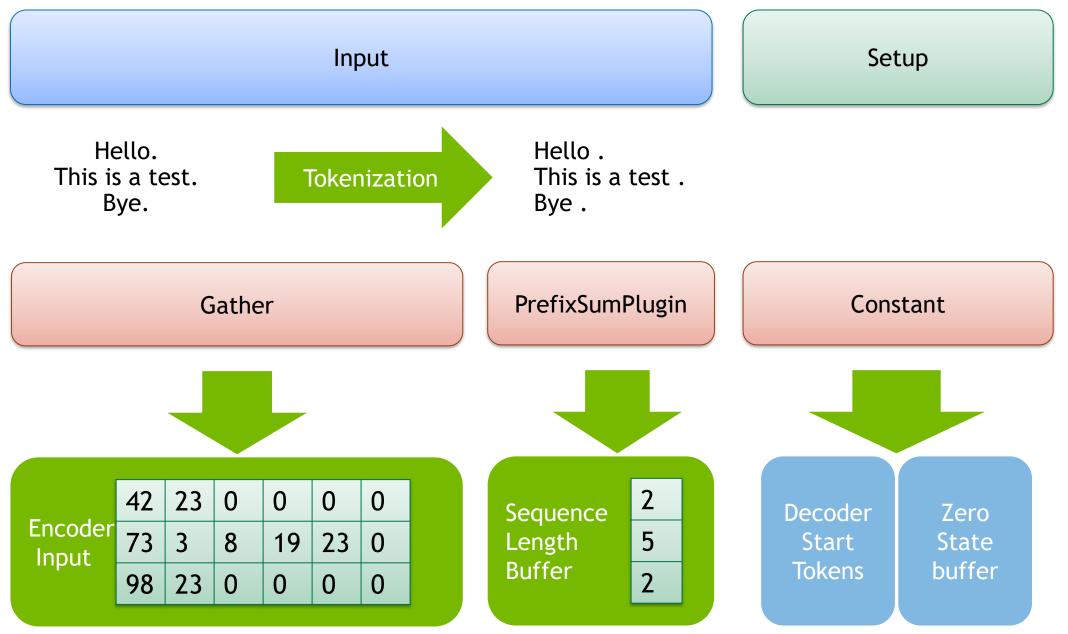


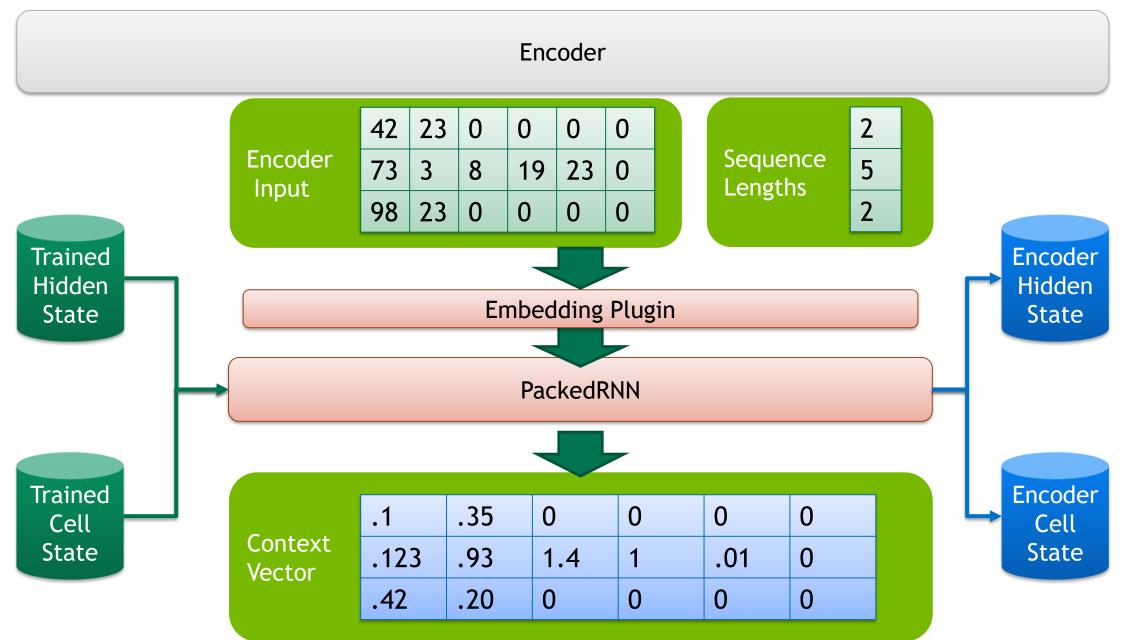
# Agenda

- What is NMT?
- What is current state?
- What are the problems?
- How did we solve it?
- What perf is possible?

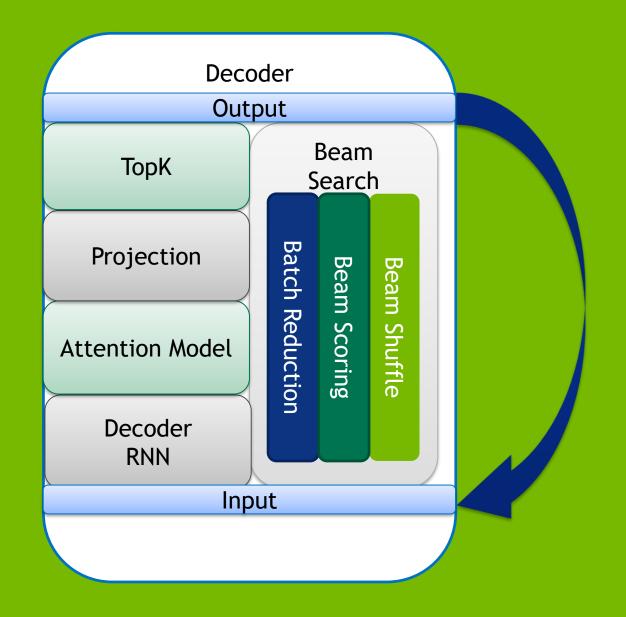
### ENCODER

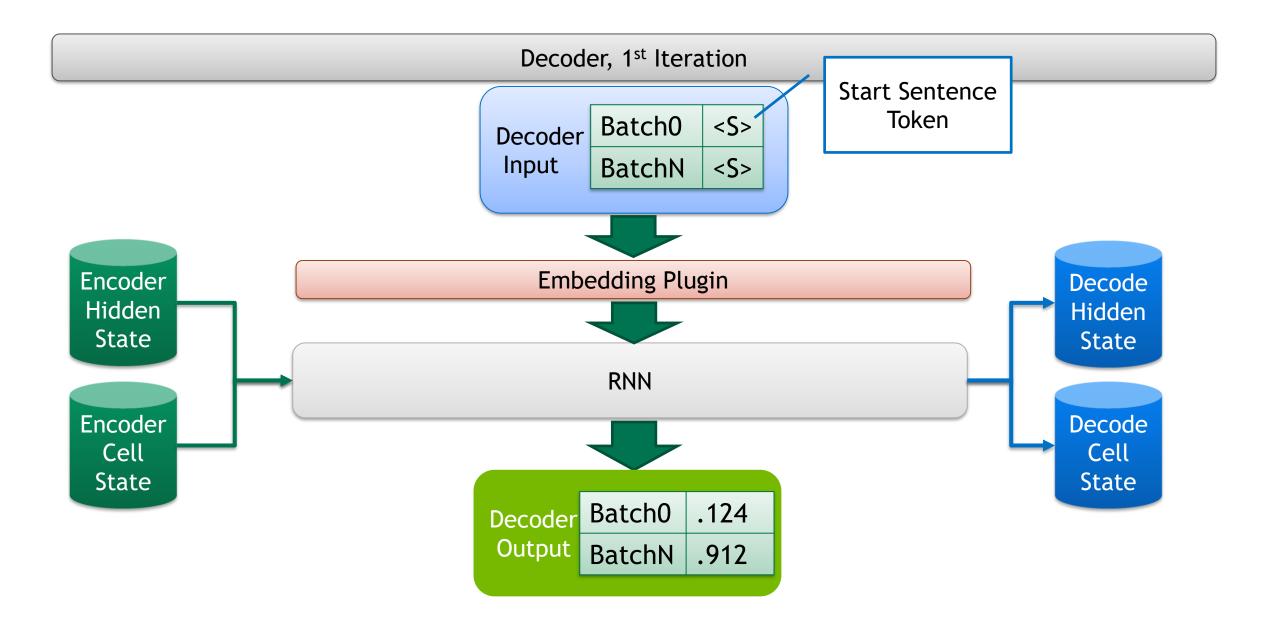


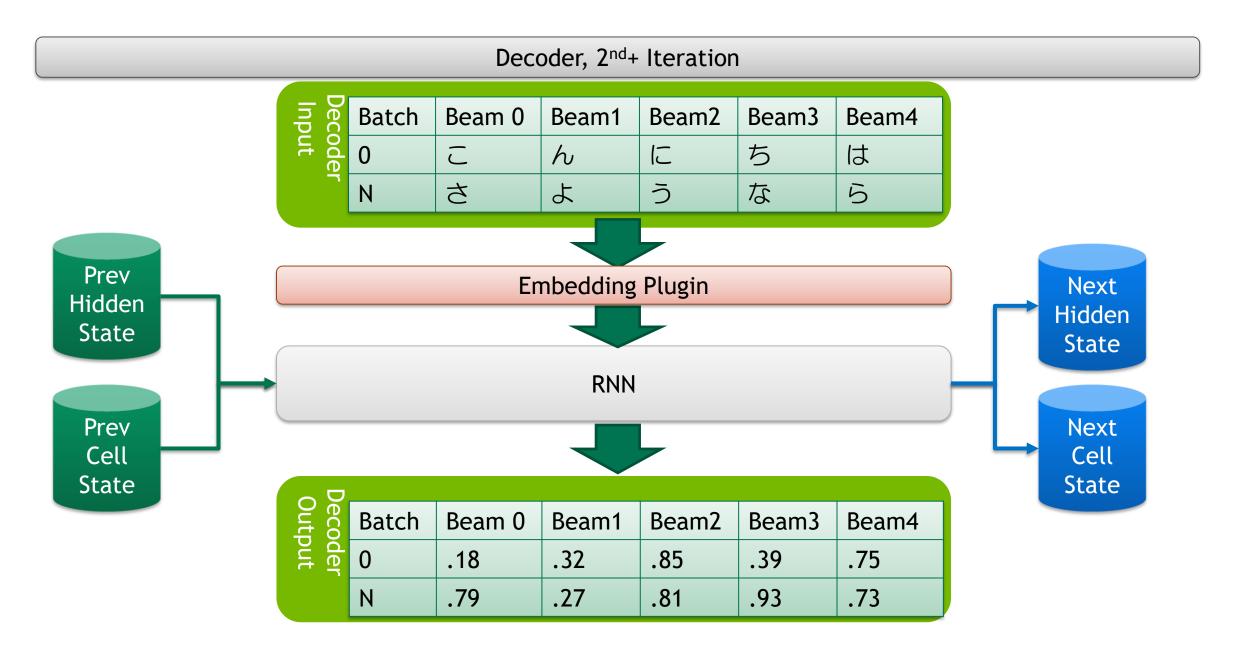




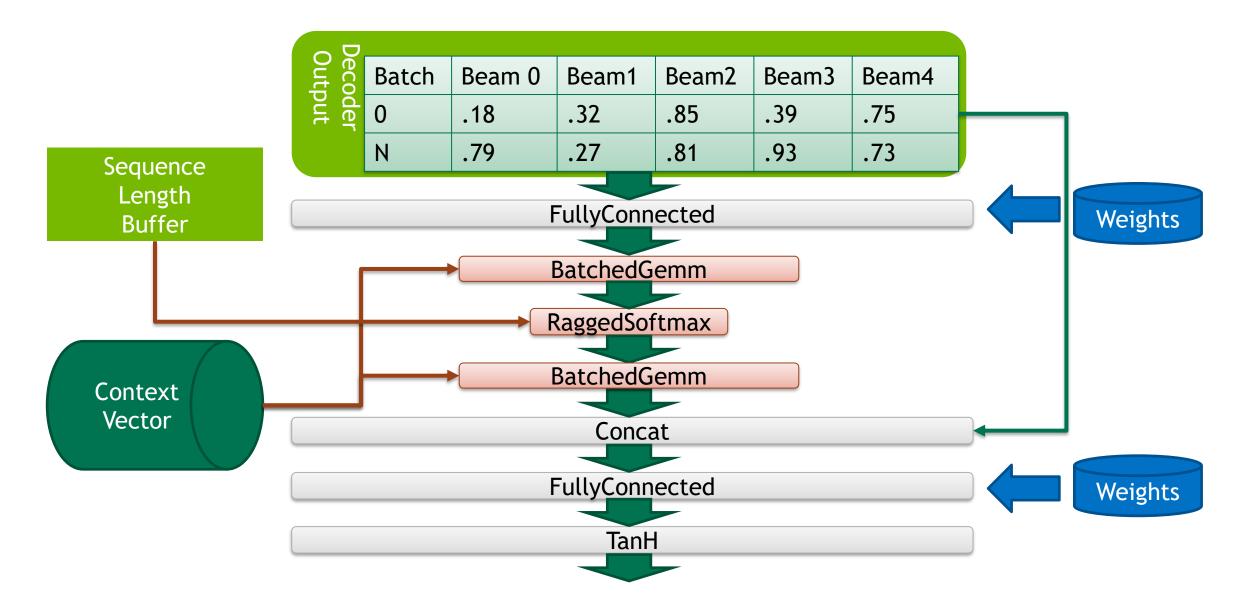
### DECODER

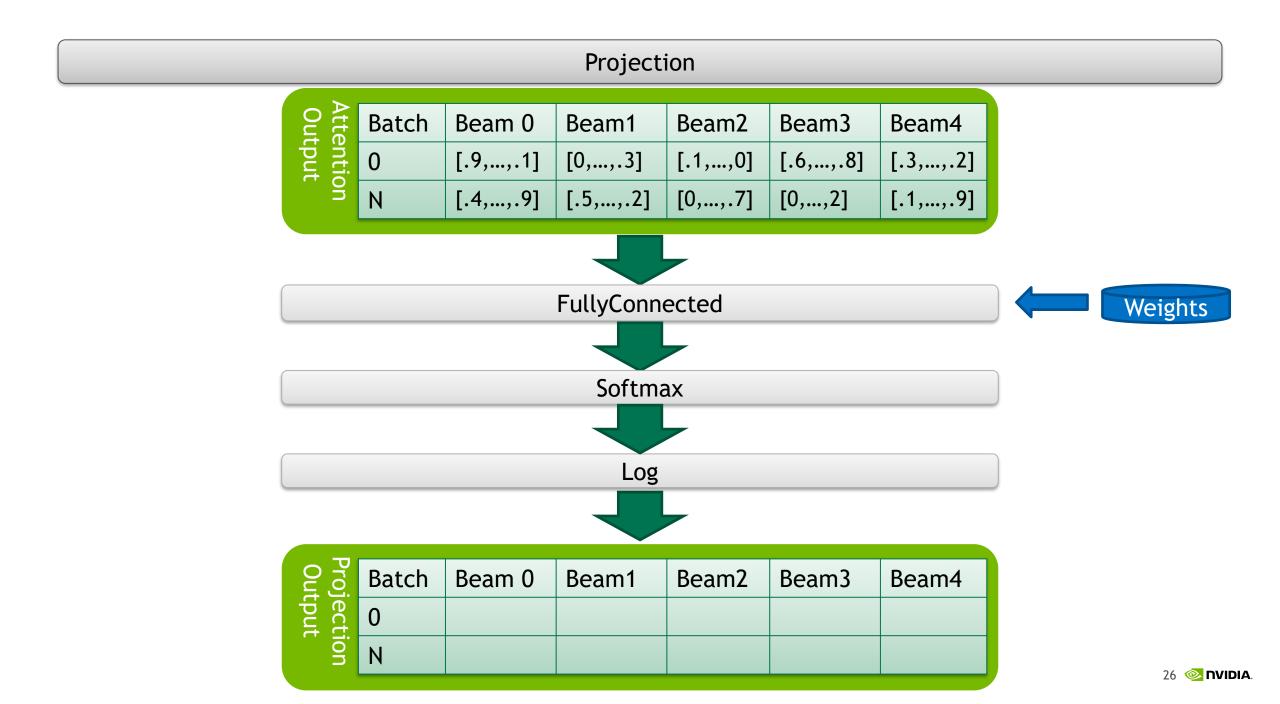


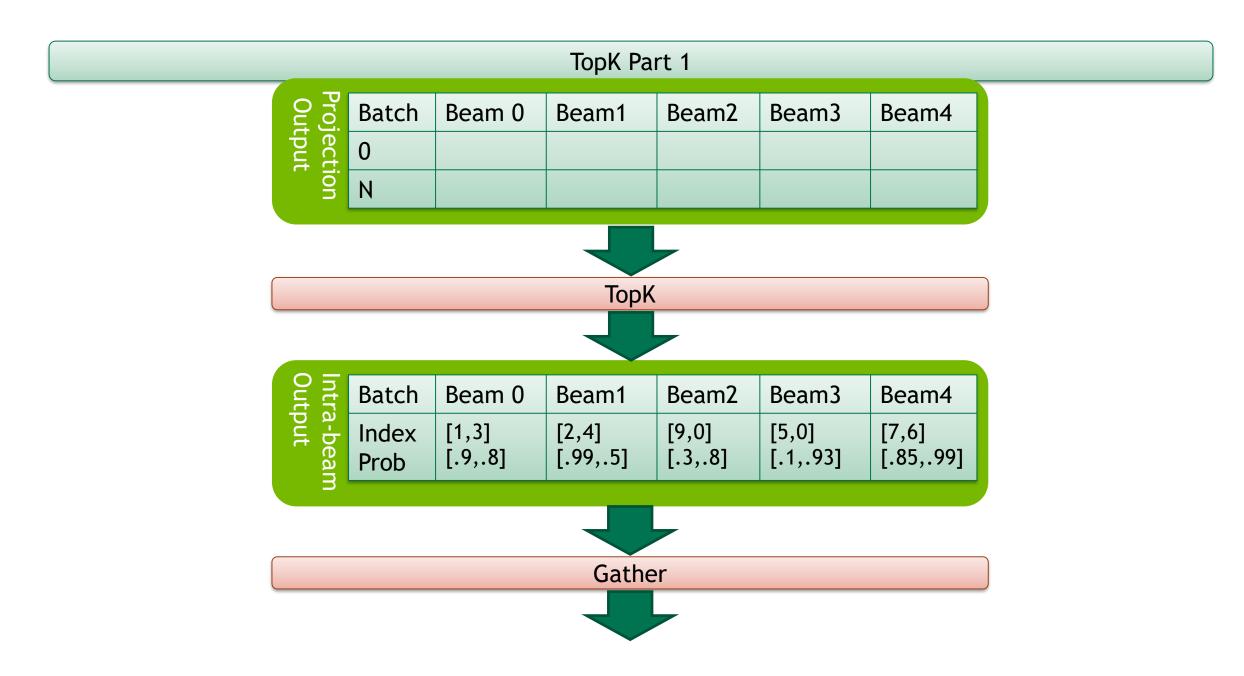


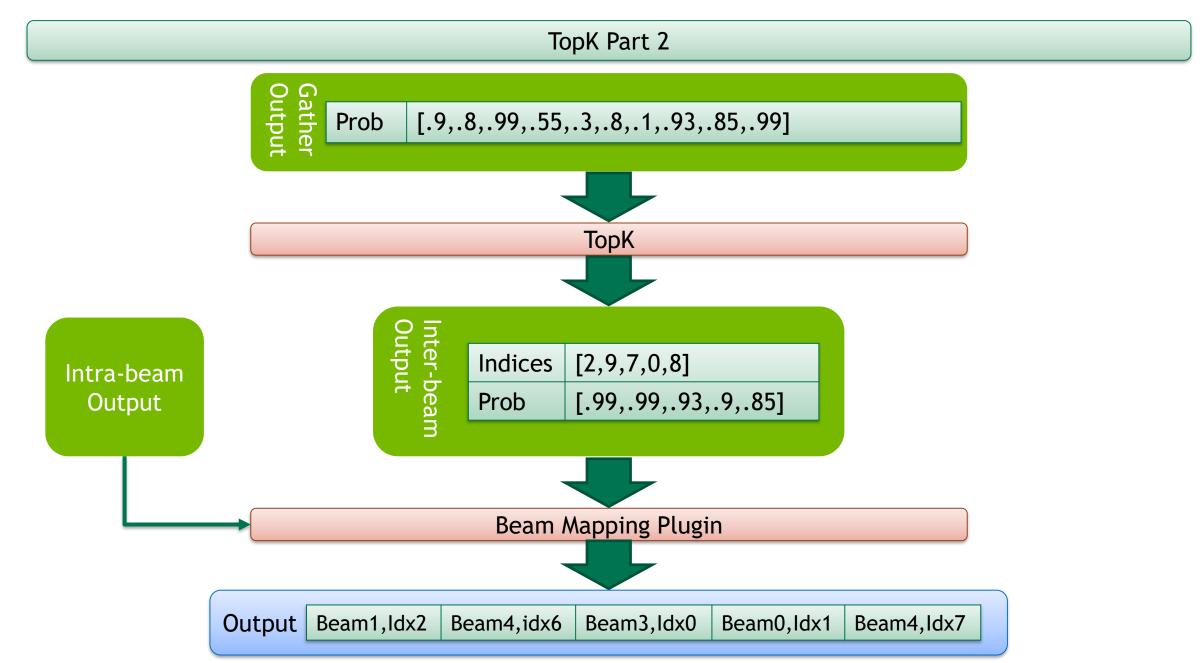


#### **Global Attention Model**

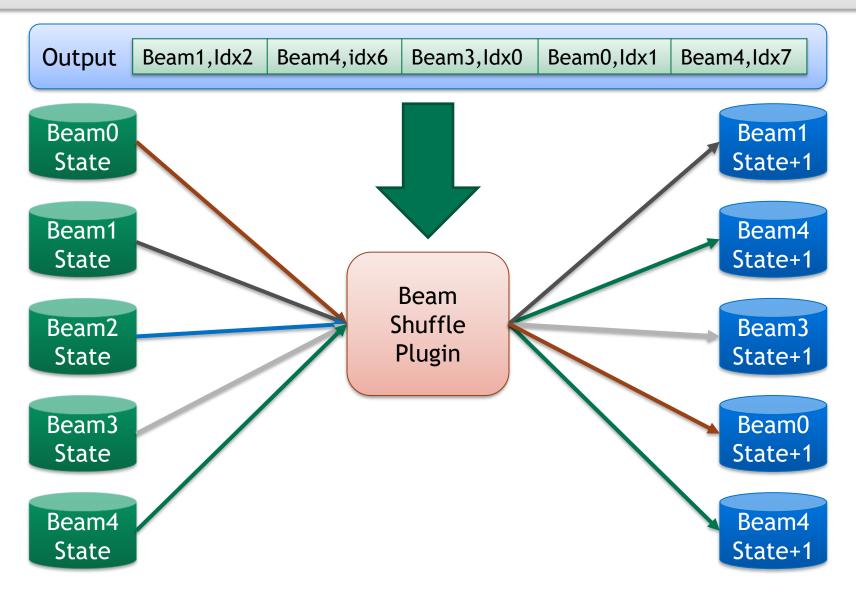




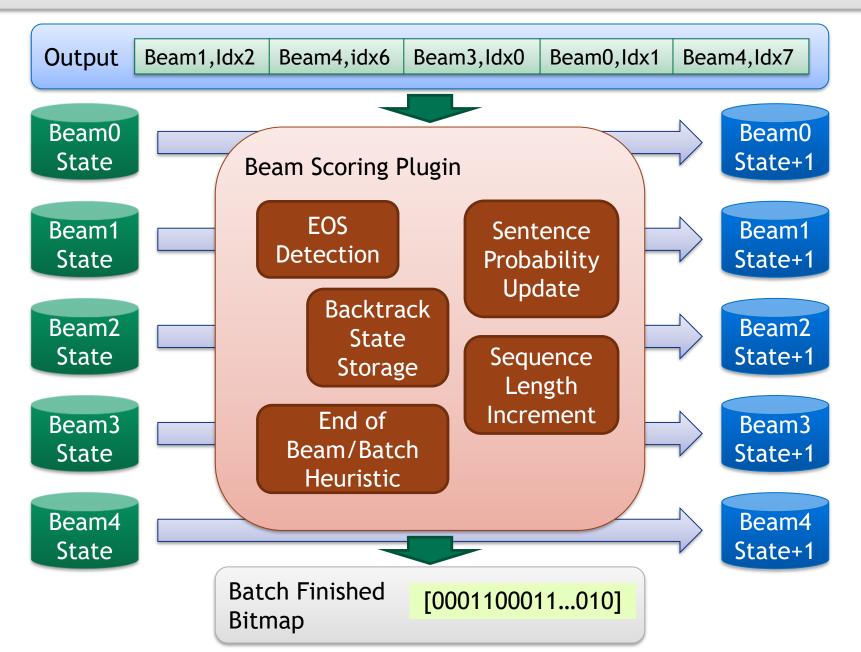




#### Beam Search - Beam Shuffle

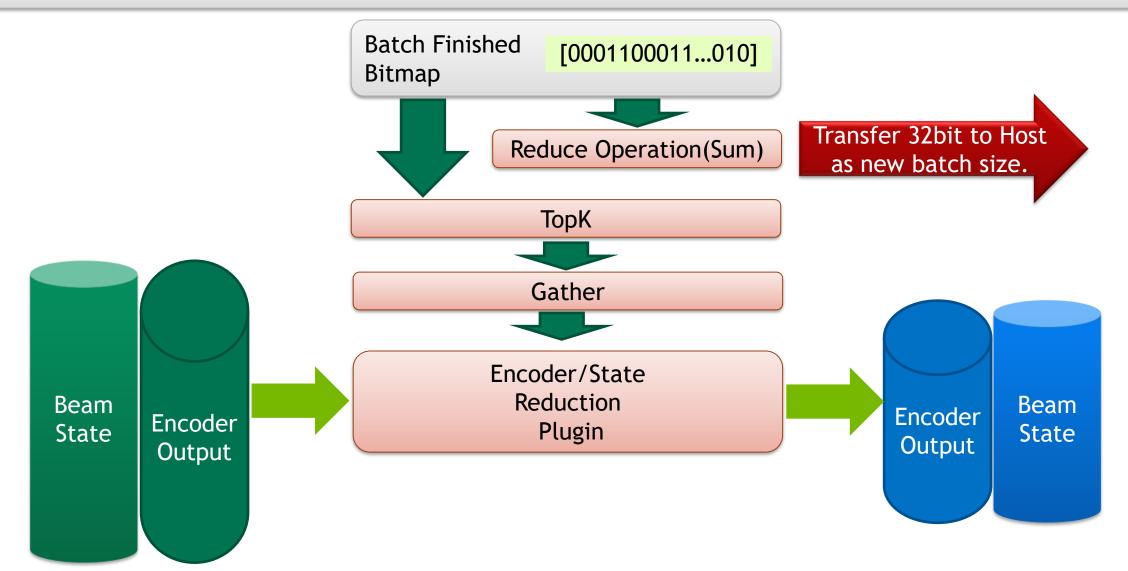


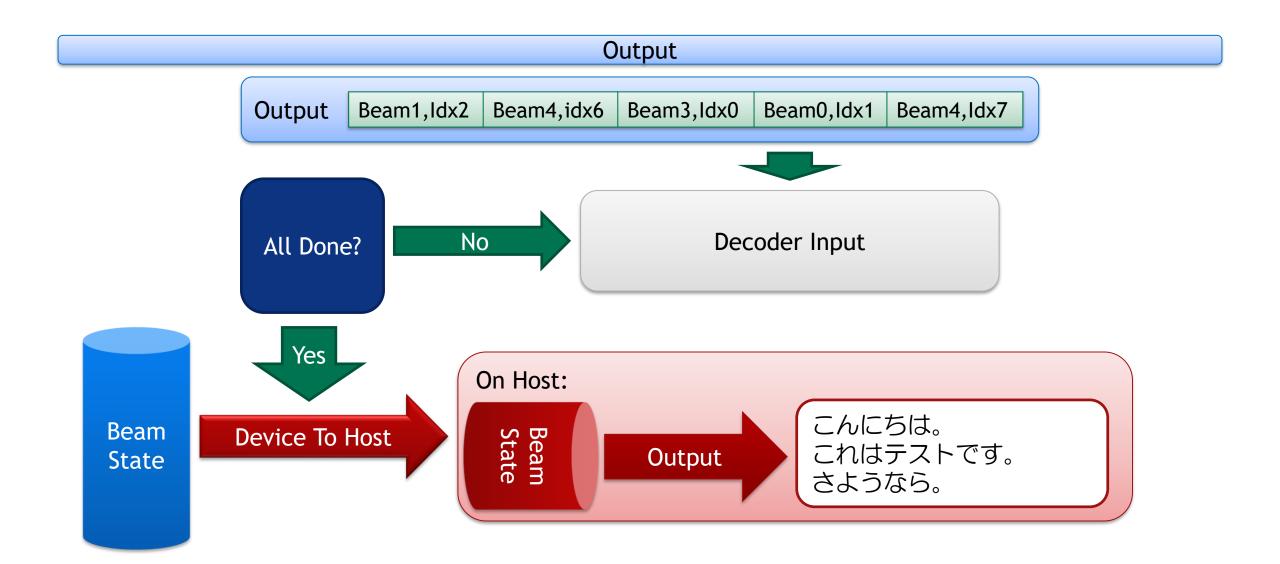
#### Beam Search - Beam Scoring



30 📀 nvidia.

#### Beam Search - Batch Reduction

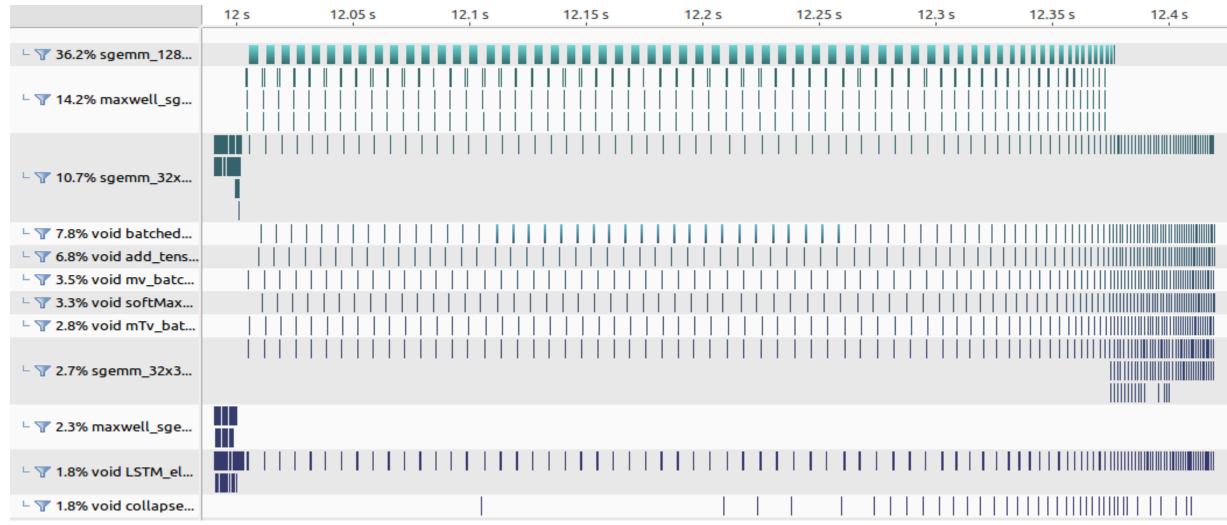




### **TENSORRT ANALYSIS**

12 s	12.05 s	12.1 s	12.15 s	12.2 s	12.25 s	12.3 s	12.35 s	12.4 s

## **TENSORRT KERNEL ANALYSIS**

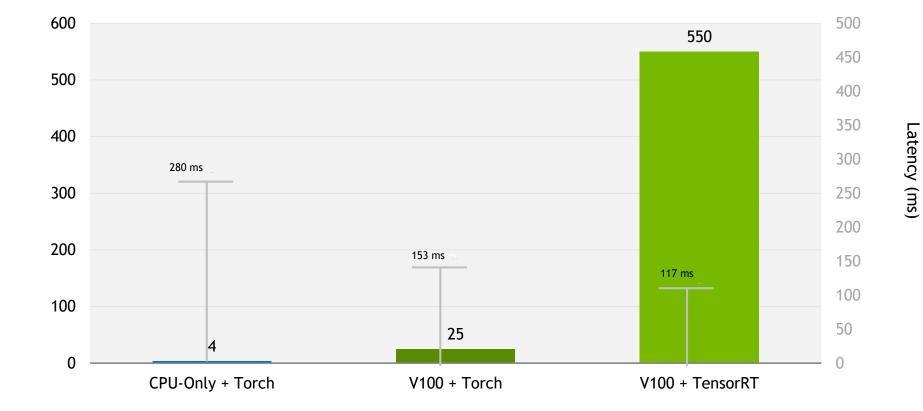


# Agenda

- What is NMT?
- What is current state?
- What are the problems?
- How did we solve it?
- What perf is possible?

### RESULTS

## 140x Faster Language Translation RNNs on V100 vs. CPU-Only Inference (OpenNMT)



Inference throughput (sentences/sec) on OpenNMT 692M. V100 + TensorRT: NVIDIA TensorRT (FP32), batch size 64, Tesla V100-PCIE-16GB, E5-2690 v4@2.60GHz 3.5GHz Turbo (Broadwell) HT On. V100 + Torch: Torch (FP32), batch size 4, Tesla V100-PCIE-16GB, E5-2690 v4@2.60GHz 3.5GHz Turbo (Broadwell) HT On. V100 + Torch: Torch (FP32), batch size 1, Intel E5-2690 v4@2.60GHz 3.5GHz Turbo (Broadwell) HT On. V100 + Torch: Torch (FP32), batch size 1, Intel E5-2690 v4@2.60GHz 3.5GHz Turbo (Broadwell) HT On. V100 + Torch: Torch (FP32), batch size 1, Intel E5-2690 v4@2.60GHz 3.5GHz Turbo (Broadwell) HT On.

## SUMMARY

- Show that topK no longer dominates sequence inference time.
- Show that RNN Inference is compute bound, not memory bound.
- TensorRT accelerates sequence inferencing.
  - Over two orders of magnitude higher throughput over CPU.
  - Latency reduction by more than half over CPU.





#### PRODUCT PAGE

developer.nvidia.com/tensorrt

## LEARN MORE

#### PRODUCT PAGE

#### developer.nvidia.com/tensorrt

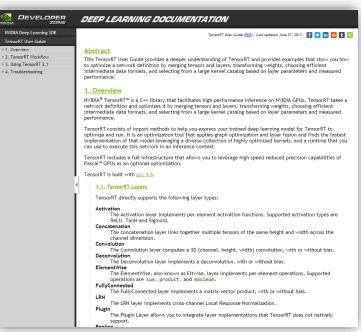
NVIDIA ACCELERATED COMPUTING Downloads Training Ecosystem F	Forums <b>Q</b> Join Logi		
NVIDIA TensorRT Programmable Inference Accelerator			
ome > ComputeWorks > Deep Learning > Software > NVIDIA TensorRT			
magna an anna	QUICKLINKS		
/IDIA TensorRT™ is a high-performance deep learning erence optimizer and runtime that delivers low	Accelerated Computing - Training		
ency, high-throughput inference for deep learning plications. TensorRT can be used to rapidly optimize,	CUDA GPUs		
idate, and deploy trained neural networks for [Click to Zoom]	Tools & Ecosystem		
renne on typer section of the sectio	OpenACC: More Science Less Programming		
inificantly reduces latency, as demanded by real-time services such as streaming video tegorization on the cloud or object detection and segmentation on embedded and automotive	CUDA FAQ		
atforms. With TensorRT developers can focus on developing novel Al-powered applications ther than performance tuning for inference deployment. TensorRT runtime ensures optimal erence performance that can meet the most demanding latency and throughput requirements.	GPU Computing		
/hat's New in TensorRT 3?	NVIDIA HPC Developer @NVIDIAHPCDev		
InsorRT 3 is the key to unlocking optimal inference riformance on Volta GPUs. It delivers up to 40k higher	In a week, register for our #webinar t deep dive into #deeplearning deployr workflow w/ TensorRT: nvda.ws/2gBj		

throughput in under 7ms real-time latency vs. CPU-Only

inference.

#### DOCUMENTATION

#### docs.nvidia.com/deeplearning/sdk



#### TRAINING

#### nvidia.com/dli



### Q&A



