

# Non-Local Lattice Encoding for Bit-Vectorized Cellular Automata GPU Implementations

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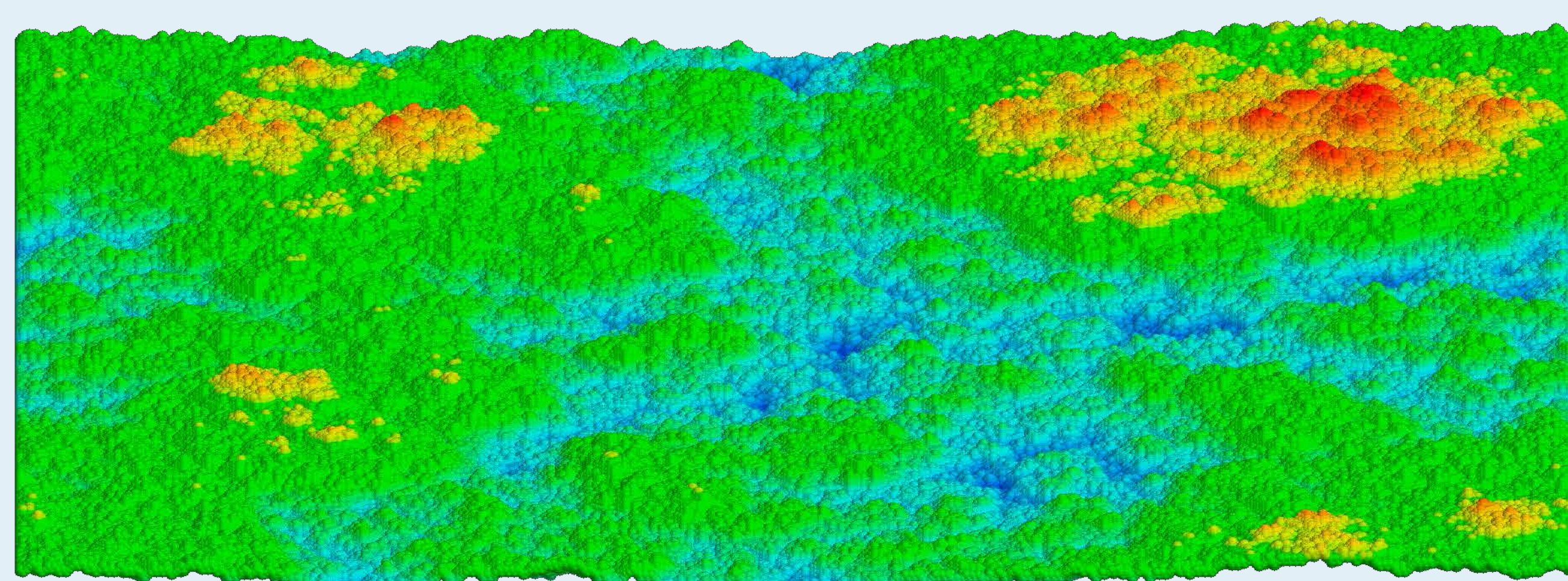
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- stochastic cellular automata are widely used
  - in combination with machine learning to predict land use change [1]
  - in magnetism for the Ising model [2]
  - for surface growth models [3] like restricted solid-on-solid model
- large scale atomistic simulations required to understand self-organization and evolution of various systems



growing surface in the steady state

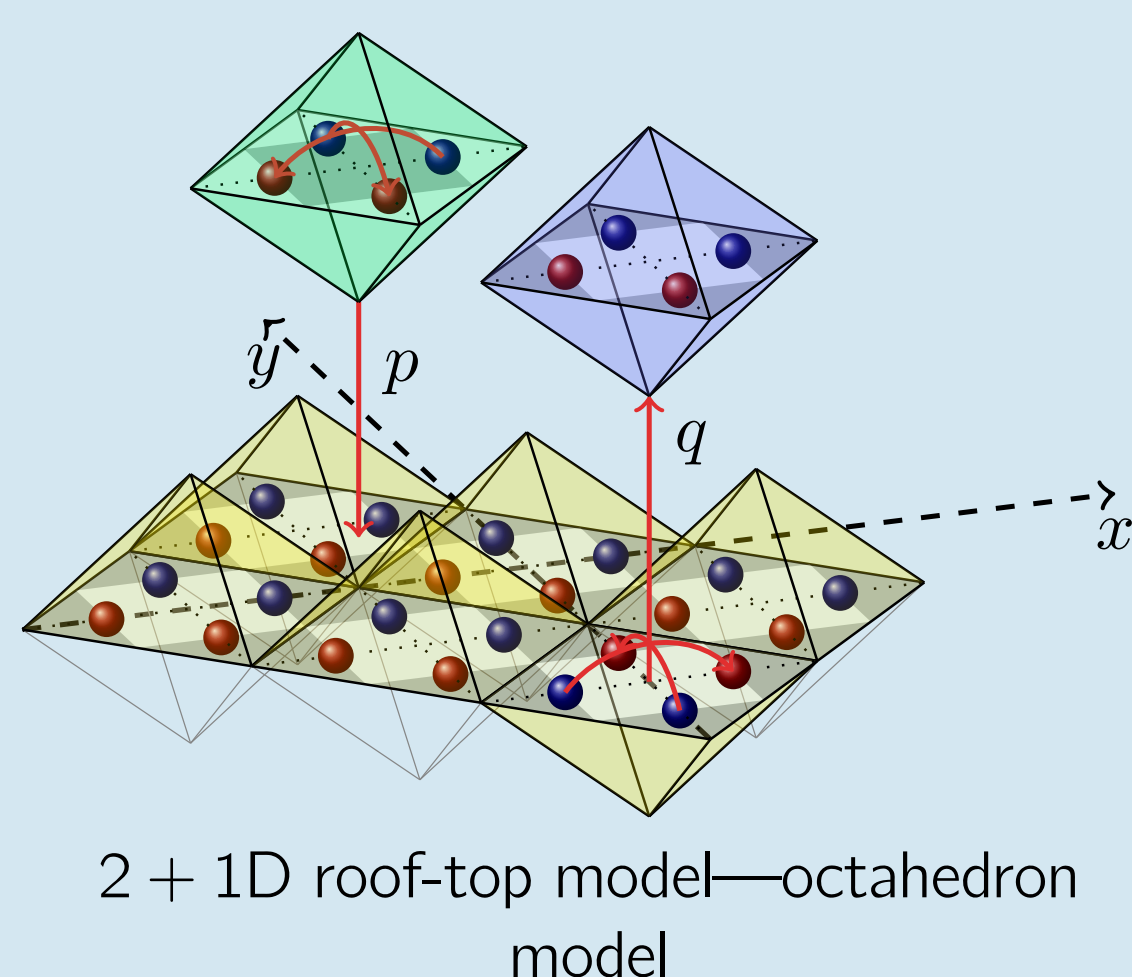
- simulating randomly growing surface with stochastic cellular automaton (SCA)
- Kardar-Parisi-Zhang (KPZ) or Edwards-Wilkinson (EW) universality class [4]
- can describe *growth processes*, directed polymers in random media, randomly stirred fluids, dissipative transport and magnetic flux lines in superconductors.

$$d_t h(\mathbf{x}, t) = \underbrace{v}_{\text{mean growth vel.}} + \underbrace{\sigma_2 \nabla^2 h(\mathbf{x}, t)}_{\text{surface tension}} + \underbrace{\lambda [\nabla h(\mathbf{x}, t)]^2}_{\text{local growth vel.}} + \underbrace{\eta(\mathbf{x}, t)}_{\text{noise}}$$

KPZ stochastic differential equation

- GPGPU enables simulations of micron-sized volumes, billions of atoms and studies of the long-time evolution of systems

## Stochastic CA for Roof-Top Model

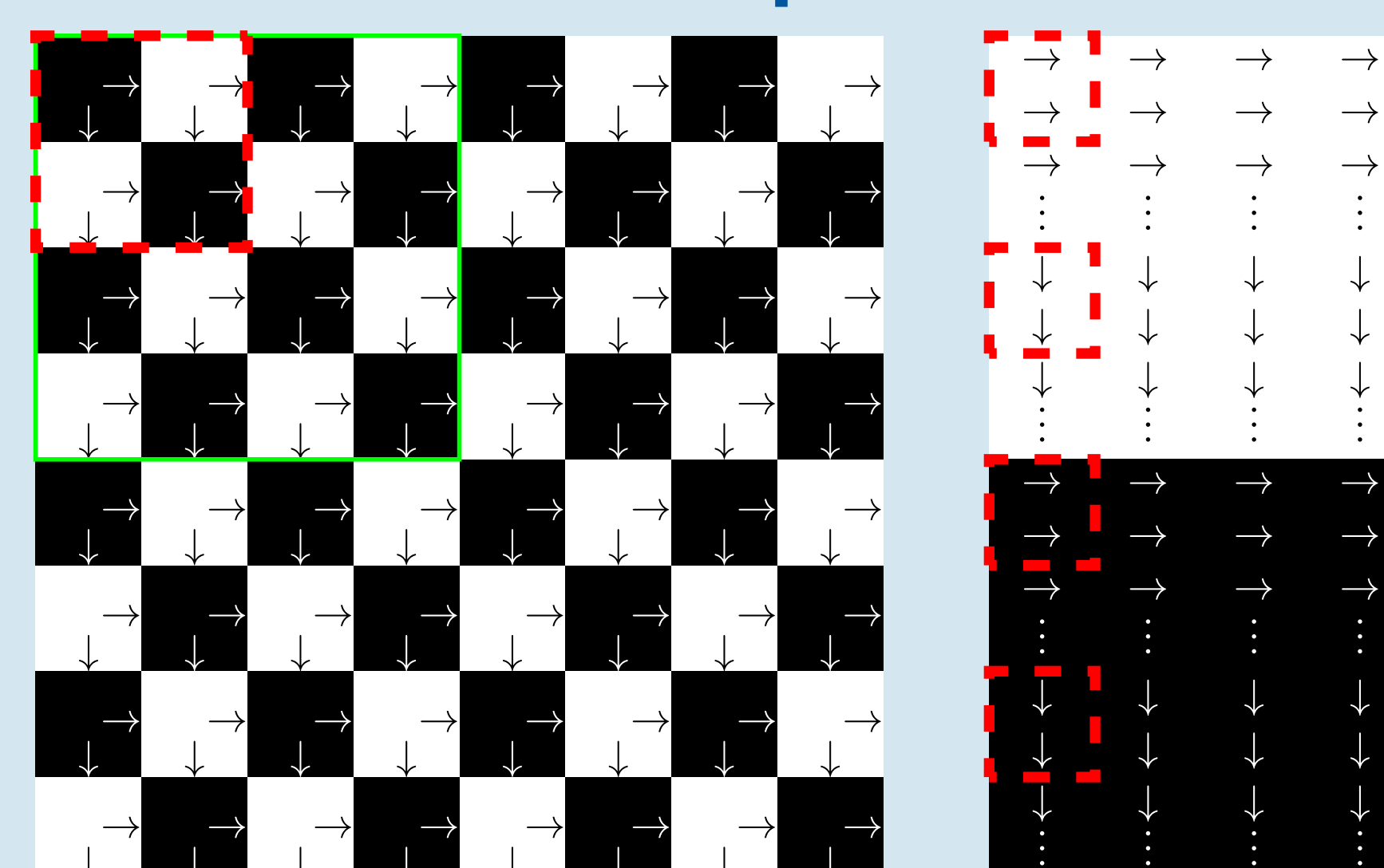


- stochastic model for surface growth [5, 6]
- 2D square lattice (octahedron model)
- carry out *random* depositions (probability  $p$ ) or removals (probability  $q$ )
- time  $t$  measured in sweeps of the lattice: Monte-Carlo-Steps (MCS)
- KPZ universality for  $q = 0$
- EW universality for  $p = q$

## Checkerboard Update Algorithm (SCA)

- bit-coded up- or down-slopes in between lattice-sites, two bits per site
- surface decomposed into checkerboard of even (white) and odd (black) lattice
- sites on the even or odd lattice, respectively, do not interact with each other during single lattice sweeps
  - update of sites on one sub-lattice can be carried out in any order
  - sub-lattices are updated in alternation

## Bit-Vectorized Implementation using Non-Local Encoding



- arrows ( $\rightarrow$ ,  $\downarrow$ ) represent slopes connecting sites
- red frames indicate corresponding data in the respective encodings

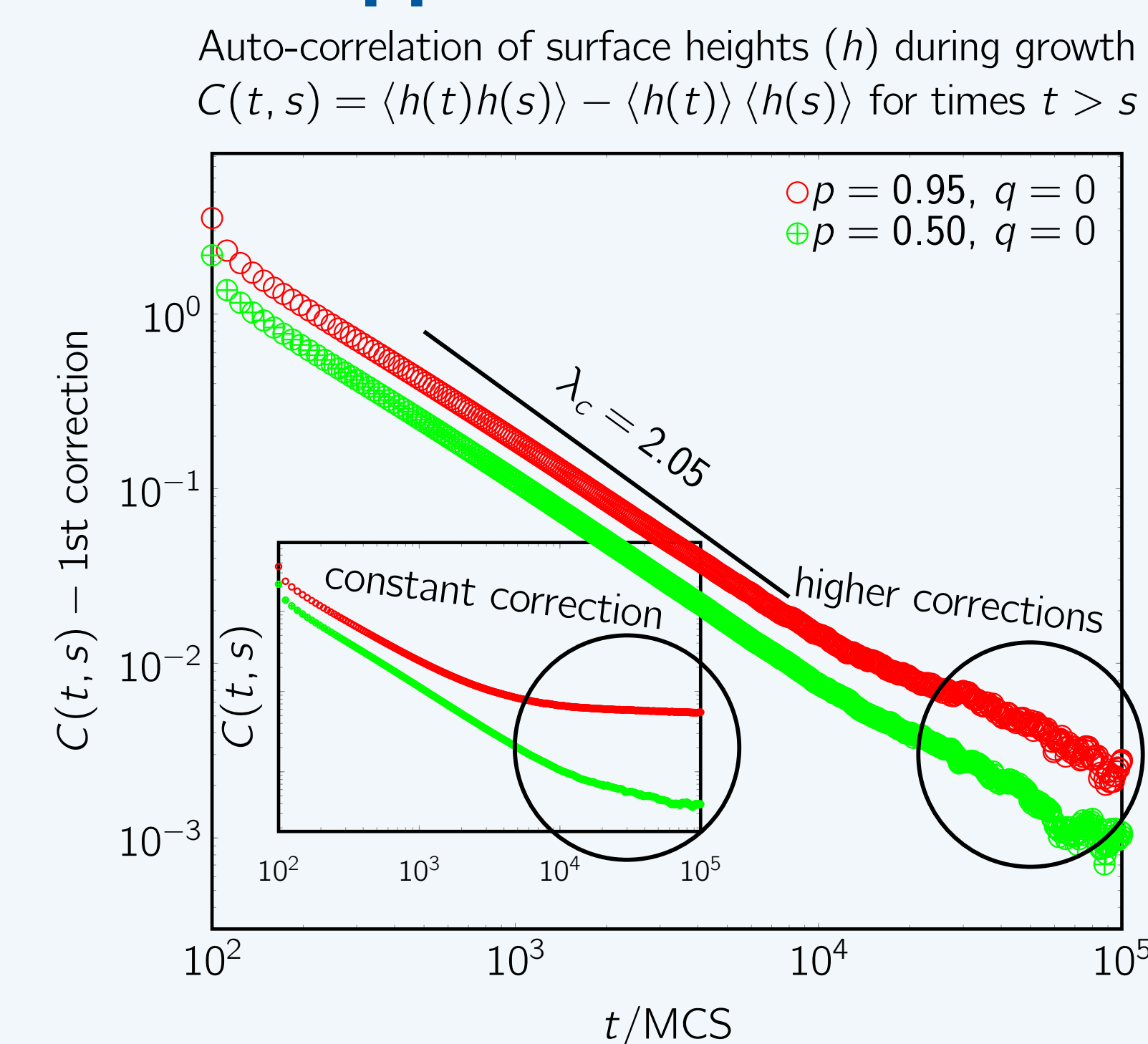
## Local $\rightarrow$ Non-Local Encoding

- in *local encoding* attributes of a lattice site are encoded *on site*, sites are ordered by physical coordinates
  - good for random site-selection, neighbors can be accessed in single memory transaction
- in *non-local encoding* same attributes of all sites are stored at consecutive addresses, sites are ordered by sub-lattice first (white: even, black: odd)
  - required for bit-level vectorization
  - reduced bandwidth overhead when updating one sublattice only

## GPU Implementation

- each thread processes chunks of 32 lattice sites (dword), neighboring in x direction on one sublattice
  - requires only one random number for 32 updates, relies on all bits being random
- block used as virtually larger word-size (larger SIMD-size)
  - data exchange between threads via shared memory, no warp shuffle.
  - $\Rightarrow$  manual caching improves memory access efficiency (100 %, except for huge systems)

## Future Application Towards Surface Aging



- stochastic surface growth can only be modelled exactly by sequential random site-selection
- SCA is widely used and more efficient
- + SCA gives correct asymptotic scaling properties
- SCA introduces strong corrections to autocorrelation properties
- ! corrections have not been studied before
  - constant correction can be extrapolated, but requires long-time runs for small  $p$
  - decreases exponentially with  $p$
  - higher corrections require much statistics and long-time runs

## Conclusions

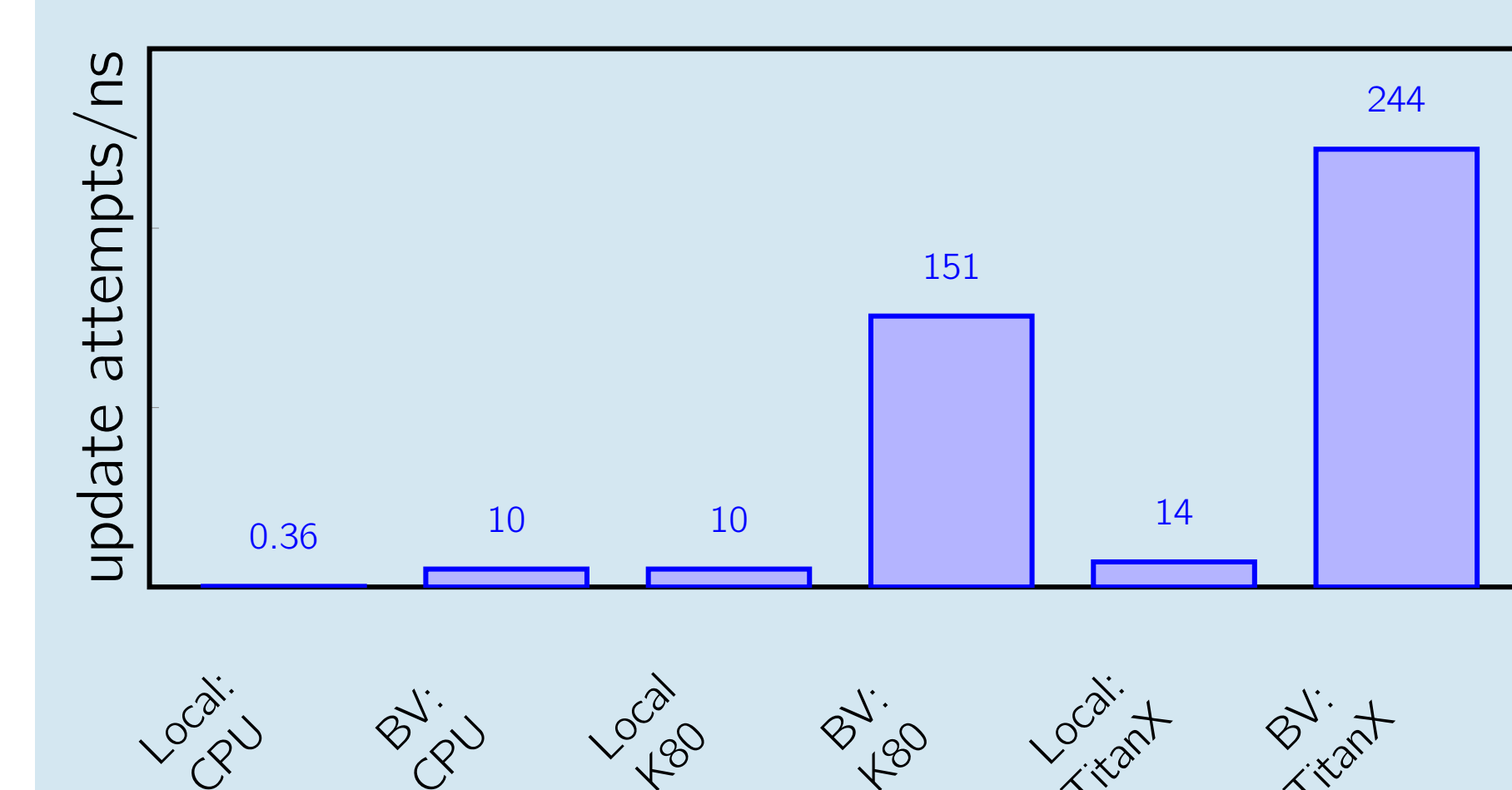
- $\sim 20\times$  speedup for bit-level vectorization over non-vectorized SCA on GPU, due to more efficient use of random numbers and global memory access
  - approach transferable to other lattice-based SCAs (and CAs)
- $\Rightarrow$  will be able to compute higher-order correlation corrections

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## Benchmarks



- Bit-vectorized (BV) CPU code uses 64-bit vectors
  - $2\times$  Xeon E5-2603 (6 Cores @1.6 GHz)
  - SSE and AVX via gcc vector extensions did not result in speedup